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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,741	KOLB ET AL.	
	Examiner	Art Unit	
	JOSEPH SCHELL	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 18* is/are allowed.

6)☒ Claim(s) *10-14 and 16* is/are rejected.

7)☒ Claim(s) *17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 10-19 have been examined.

Claims 15 and 18 are allowable.

Claims 17 and 19 have been objected to as containing allowable subject matter, yet dependant upon rejected base claims.

Claims 10-14 and 16 have been rejected.

Response to Arguments

1. The arguments submitted January 22, 2008 have been fully considered but are not persuasive.

2. Regarding Claim 10, Applicant argues that Tsai ('196) does not disclose the copy being stored in a different address area of the same microcomputer. The examiner respectfully disagrees. Tsai ('196) column 2 lines 28-31 teaches this aspect.

3. Regarding Claim 13, Applicant argues that the claim is not obvious over the prior art because the prior art does not teach two microcomputers within a sensor circuit of a motor vehicle. The examiner respectfully disagrees and asserts that the combination of Corrie ('635) in view of Hosaka ('594) does teach the broadest reasonable interpretation of the claim.

Applicant appears to argue that the limitation of "two microprocessors that are each located within a sensor circuit" necessitates that the microprocessors be physically surrounded by sensor-functioning micro-electronics.

The broadest reasonable interpretation of a "sensor circuit" is circuitry that measures a physical quantity and converts it into an electrical signal. To say that a microprocessor is located within a circuit does not require that the microprocessor be used by the sensor function, nor does it require that the microprocessor share the same PCB or be otherwise physically adjacent to the sensor functions.

The broadest reasonable interpretation of this limitation of "located within a sensor circuit" is therefore that the microprocessor is operably connected to the sensor-specific hardware. The circuit is created by the microprocessor sinking sensor-related electrical signals. Any additional limitations to be inferred from the limitation need to either be added to the claim or argued in detail.

Allowable Subject Matter

4. Claims 15 and 18 are allowable.

Claims 17 and 19 are objected to as containing allowable subject matter while being dependent on rejected base claims.

The allowable subject matter in these claims is as stated in the office action of March 28, 2007.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai ('196) in view of Hosaka ('594).

6. As per claim 10, Tsai ('196) discloses a method for monitoring program execution in a microcomputer, comprising the steps of:

executing, by the microcomputer, a program including processing input data and generating first output data (column 9 lines 38-41);

executing a copy of the program with the input data intended for the program and generating a second output data, the copy being stored in a different address area of the microcomputer than the program in the microcomputer (see abstract, there are multiple copies of a target program and user-specified variables are compared between the copies, also see column 2 lines 29-31 wherein both copies are within a single machine); and

comparing the second output data from the copy with the first output data from the program and generating an error message if the second output data from the copy do not match the first output data from the program (see abstract, on a mismatch a new copy of a program is restarted from a previous checkpoint).

Tsai ('196) does not expressly disclose the system for use in a sensor circuit for sensing at least one operating parameter of a motor vehicle.

Hosaka ('594) teaches a vehicle engine control system that uses redundant processors for backup operation while measuring and displaying various vehicle driving information (column 1 lines 29-37).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify redundant program system such that it is used for a vehicle sensor circuit as disclosed by Hosaka ('594). This modification would have been obvious because error detecting and tolerance within such a sensor system allows for continued safe operation of the vehicle (Hosaka ('594), end of abstract).

7. As per claim 11, Tsai ('196) in view of Hosaka ('594) discloses the method of claim 10, further comprising the step of further executing the copy for processing prescribed test data and generating third output data from the prescribed test data, comparing the third output data generated from the prescribed test data with

comparative data stored in a memory, and generating an error message if the third output data generated from the prescribed test data do not match the comparative data (Tsai ('196) column 8 lines 43-45, at each breakpoint each backend reports preselected variable values to the front end for comparison. Considering that there are three copies of the target program, one per backend machine, upon the second breakpoint and variable comparison, the second copy of the target program generates a third output data from the second copy of the program).

8. As per claim 12, Tsai ('196) in view of Hosaka ('594) discloses the method of claim 10, further comprising the steps of one of setting or changing a respective flag following the execution of program portions of the program, and generating an error message if not all the flags have been set or changed following the execution of the program (Tsai ('196) column 10 lines 58-61, each set breakpoint is a flag, and when the breakpoint is not reached by the target program a error is declared).

9. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corrie ('635) in view of Hosaka ('594).

10. As per claim 13 Corrie ('635) discloses a method for monitoring the program execution in at least two interconnected microcomputers (paragraph 11, master and slave processors), comprising the steps of:

generating, by one of the microcomputers, a request which is transmitted to the other microcomputer (paragraph 11);

using, by the other of the microcomputers, prescribed input data to prompt the execution of a program in response to receipt of the request (paragraph 11);

returning, by the other of the microcomputers, a response which is dependent on the input data to the one of the microcomputers (paragraph 11, the unit for receiving and unit for comparing are associated with the master processor);

comparing, in the one of the microcomputers, the request and the response with one another (paragraph 11, the unit for receiving and unit for comparing are associated with the master processor); and

generating an error message if the request does not match the response (paragraph 30).

Corrie ('635) does not expressly disclose the method wherein the two interconnected microcomputers are in a sensor circuit sensing at least one operating parameter of a motor vehicle.

Hosaka ('594) teaches a vehicle engine control system that uses redundant processors for backup operation while measuring and displaying various vehicle driving information (column 1 lines 29-37).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify redundant program system such that it is used for a vehicle sensor circuit as disclosed by Hosaka ('594). This modification would have been obvious because error detecting and tolerance within such a sensor system allows for continued safe operation of the vehicle (Hosaka ('594), end of abstract).

11. As per claim 14, Corrie ('635) in view of Hosaka ('594) discloses the method of claim 13, wherein the program is a copy of another program that performs a function of the other of the microcomputers (as shown in Corrie ('635) Figure 1, the master and slave processors are remotely located. Also see Corrie ('635) paragraph 39).

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrie ('635) in view of Hosaka ('594) and in further view of Alderson ('649).

Corrie ('635) in view of Hosaka ('594) discloses the method of claim 13. Corrie ('635) in view of Hosaka ('594) does not disclose the method of claim 13, further comprising the steps of one of setting or changing, within the other of the microcomputers, a respective flag in a flag register following the execution of program portions of the program, and generating an error message if not all the flags have been set or changed following the execution of the program.

Alderson ('649) teaches a system that traces program functions and consolidates the trace information from each function into a single block (see abstract and figure 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the program monitoring system disclosed by Corrie ('635) in view of Hosaka ('594) such that program tracing is performed and the traced data consolidated into a single block. This modification would have been obvious because tracing allows a programmer to closely follow and analyze the state of a system around the time of a fault (Alderson ('694) column 1 lines 12-15) while the consolidation allows for multiple functions to be ordered according to a global event timeline (Alderson ('694) column 2 lines 13-16).

Wikipedia's Memory Hierarchy provides an overview of different kinds of memory in terms of their relative speeds and their implementations in modern CPUs.

At the time of invention it would have been further obvious to a person of ordinary skill in the art to modify the program monitoring system disclosed by Corrie ('635) in view of Hosaka ('594) and Alderson ('649) such that the traced data is stored in a register. This modification would have been obvious because CPU registers are the fastest form of memory (see Memory Hierarchy).

Finally, the examiner takes official notice that it would be obvious to modify the system disclosed by Corrie ('635) in view of Hosaka ('594), Alderson ('649) and Wikipedia's Memory Hierarchy such that a error message is generated if tracing is not completed. An error message feature is well known in the art and is especially appropriate in view of the "trace complete" message provided by Alderson ('649) (column 5 lines 29-32). See also the reference, Wikipedia's Error Message.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH SCHELL whose telephone number is (571)272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

JS